Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

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1. (**Currently Amended**) A liquid crystal display device having a plurality of pixels, wherein the plurality of pixels respectively ~~have~~ comprise:

a plurality of storage circuits;

a write-in storage circuit selection portion electrically connected to a selected one of the plurality of storage circuits;

a read storage circuit selection portion electrically connected to a selected one of the plurality of storage circuits;

a write-in transistor electrically connected to the write-in storage circuit selection portion;

a read transistor electrically connected to the read storage circuit selection portion; and

a liquid crystal element electrically connected to the read transistor.

2. (**Previously Presented**) A device according to claim 1, wherein the storage circuit is a static memory (SRAM).

3. (**Previously Presented**) A device according to claim 1, wherein the storage circuit is a ferroelectric memory (FeRAM).

4. (**Previously Presented**) A device according to claim 1, wherein the storage circuit is a dynamic memory (DRAM).

5. (**Previously Presented**) A device according to claim 1, wherein the storage circuit is formed on a glass substrate.

6. (**Previously Presented**) A device according to claim 1, wherein the storage circuit is formed on a plastic substrate.

7. (**Previously Presented**) A device according to claim 1, wherein the storage circuit is formed on a stainless substrate.

8. (**Previously Presented**) A device according to claim 1, wherein the storage circuit is formed on a monocrystalline wafer substrate.

9. (**Original**) An electronic device using a liquid crystal display device according to claim 1.

10. (**Previously Presented**) A method according to claim 9, wherein the electronic device is selected from the group consisting of a television, a personal computer, a portable terminal, a video camera or a head mount display.

11. (**Currently Amended**) A liquid crystal display device having a plurality of pixels, wherein the plurality of pixels respectively ~~have~~ comprise:

n x m storage circuits for storing m frames (m is an integer, where 1 ≤m) of an n bit digital image signal (n is an integer, where 2 ≤n);

a write-in storage circuit selection portion electrically connected to a selected one of the n x m storage circuits;

a read storage circuit selection portion electrically connected to a selected one of the n x m storage circuits;

a write-in transistor electrically connected to the write-in storage circuit selection portion;

a read transistor electrically connected to the read storage circuit selection portion; and

a liquid crystal element electrically connected to the read transistor.

12. **(Previously Presented)** A device according to claim 11, wherein the storage circuit is a static memory (SRAM).

13. **(Previously Presented)** A device according to claim 11, wherein the storage circuit is a ferroelectric memory (FeRAM).

14. **(Previously Presented)** A device according to claim 11, wherein the storage circuit is a dynamic memory (DRAM).

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15. **(Previously Presented)** A device according to claim 11, wherein the storage circuit is formed on a glass substrate.

16. **(Previously Presented)** A device according to claim 11, wherein the storage circuit is formed on a plastic substrate.

17. **(Previously Presented)** A device according to claim 11, wherein the storage circuit is formed on a stainless substrate.

18. **(Previously Presented)** A device according to claim 11, wherein the storage circuit is formed on a monocrystalline wafer substrate.

19. **(Original)** An electronic device using a liquid crystal display device according to claim 11.

20. (**Previously Presented**) A method according to claim 19, wherein the electronic device is selected from the group consisting of a television, a personal computer, a portable terminal, a video camera or a head mount display.

21. (**Currently Amended**) A liquid crystal display device having a plurality of pixels, each of the plurality of pixels comprising:

a source signal line;

n write-in gate signal lines (n is an integer, where 2 ≤**[[5]]** n);

n read gate signal lines;

n write-in transistors, gate electrodes of the n write-in transistors being respectively electrically connected to any one of the different n write-in gate signal lines;

n read transistors, gate electrodes of the n read transistors being respectively electrically connected to any one of the different n read gate signal lines;

n x m storage circuits for storing m frames (m is an integer, where 1 ≤m) of an n bit digital image signal;

n write-in storage circuit selection portions;

n read storage circuit selection portions having m signal output portions, respectively; and

a liquid crystal element,

wherein one of a source and a drain region of the n write-in transistor is electrically connected to a source signal line, and the other is electrically connected to any one of the different signal input portions of the n write-in storage circuit selection portions;

wherein and the m signal output portions respectively are electrically connected to signal input portions of the different m storage circuits;

wherein the m signal input portions respectively are electrically connected to the signal output portions of the different m storage circuits; and

wherein one of the source region and the drain region of n read transistors is electrically connected to any one of the different signal output portions of the n read storage circuit selection portions, and the other is electrically connected to one electrode of the liquid crystal element.

22. (**Original**) A device according to claim 21, wherein the write-in storage circuit selection portion selects any one of m storage circuits, and becomes in continuity with one of a source region or a drain region of the write-in transistor to thereby write in the digital image signal to the storage circuit, and

wherein the read storage circuit selection portion selects any one of the storage circuits storing the digital image signal, and becomes in continuity with one of a source region or a drain region of the read transistor to thereby read the digital image which is stored.

23. (**Original**) A device according to claim 21, further comprising:

a shift register which sequentially outputs a sampling pulse according to a clock signal and a start pulse;

a first latch circuit holding n bit digital image signals (n is an integer, where $2 \leq n$) according to the sampling pulse;

a second latch circuit to which the n bit digital image signals held in the first latch circuit are transferred; and

a bit signal selection switch which selects in order by each bit the n bit digital image signals transferred to the second latch circuit, and then outputs to the source signal line.

24. (**Previously Presented**) A device according to claim 21, wherein the storage circuit is a static memory (SRAM).

25. (**Previously Presented**) A device according to claim 21, wherein the storage circuit is a ferroelectric memory (FeRAM).

26. (**Previously Presented**) A device according to claim 21, wherein the storage circuit is a dynamic memory (DRAM).

27. (**Previously Presented**) A device according to claim 21, wherein the storage circuit is formed on a glass substrate.

28. (**Previously Presented**) A device according to claim 21, wherein the storage circuit is formed on a plastic substrate.

29. (**Previously Presented**) A device according to claim 21, wherein the storage circuit is formed on a stainless substrate.

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30. (**Previously Presented**) A device according to claim 21, wherein the storage circuit is formed on a monocrystalline wafer substrate.

31. (**Original**) An electronic device using a liquid crystal display device according to claim 21.

32. (**Previously Presented**) A method according to claim 31, wherein the electronic device is selected from the group consisting of a television, a personal computer, a portable terminal, a video camera or a head mount display.

33. (**Original**) A liquid crystal display device having a plurality of pixels, each of the plurality of pixels comprises:

n source signal lines (n is an integer, where 2 $\leq$n);

a write-in gate signal line;

n read gate signal lines;

n write-in transistors;

n read transistors;

n x m storage circuits for storing m frames (m is an integer, where 1 ≤m) of an n bit digital image signal;

n write-in storage circuit selection portions;

n read storage circuit selection portions; and

a liquid crystal element,

wherein gate electrodes of n write-in transistors are respectively electrically connected to the write-in gate signal lines, one of a source region and a drain region is electrically connected to any one of the different n source signal lines and the other is electrically connected to any one of the different signal input portions of the n write-in storage circuit selection portions,

wherein the n write-in storage circuit selection portions respectively have m signal output portions, and the m signal output portions respectively are electrically connected to signal input portions of the different m storage circuits,

wherein the n read storage circuit selection portions respectively have m signal input portions, and the m signal input portions respectively are electrically connected to the signal output portions of the different m storage circuits, and

wherein gate electrodes of the n read transistors respectively are electrically connected to any one of the different n read gate signal lines, one of the source region and the drain region is electrically connected to any one of the different signal output portions of the n read storage circuit selection portions, and the other is electrically connected to one electrode of the liquid crystal element.

34. **(Original)** A device according to claim 33, wherein the write-in storage circuit selection portion selects any one of m storage circuits, and becomes in continuity with one of a source region or a drain region of the write-in transistor to thereby write in the digital image signal to the storage circuit; and

wherein the read storage circuit selection portion selects any one of the storage circuits storing the digital image signal, and becomes in continuity with one of a source region or a drain region of the read transistor to thereby read the digital image which is stored.

35. (**Original**) A device according to claim 33, further comprising:

a first latch circuit holding the 1 bit digital image signal from among n bit digital image signals (n is an integer, where 2 $\leq$n) according to the sampling pulse; and

a second latch circuit to which the 1 bit digital image signal held in the first latch circuit is transferred, and which outputs the 1 bit digital image signal to the source signal line.

36. (**Original**) A device according to claim 33, further comprising:

a shift register which sequentially outputs a sampling pulse according to a clock signal and a start pulse; and

a first latch circuit holding a 1 bit digital image signal from among n bit digital image signals (n is an integer, where 2 $\leq$n) according to the sampling pulse, and outputs the 1 bit digital image signal to the source signal line.

37. (**Previously Presented**) A device according to claim 33, wherein the storage circuit is a static memory (SRAM).

38. (**Previously Presented**) A device according to claim 33, wherein the storage circuit is a ferroelectric memory (FeRAM).

39. (**Previously Presented**) A device according to claim 33, wherein the storage circuit is a dynamic memory (DRAM).

40. (**Previously Presented**) A device according to claim 33, wherein the storage circuit is formed on a glass substrate.

41. (**Previously Presented**) A device according to claim 33, wherein the storage circuit is formed on a plastic substrate.

42. (**Previously Presented**) A device according to claim 33, wherein the storage circuit is formed on a stainless substrate.

43. (**Previously Presented**) A device according to claim 33, wherein the storage circuit is formed on a monocrystalline wafer substrate.

44. (**Original**) An electronic device using a liquid crystal display device according to claim 33.

45. (**Previously Presented**) A method according to claim 44, wherein the electronic device is selected from the group consisting of a television, a personal computer, a portable terminal, a video camera or a head mount display.

46. (**Currently Amended**) A method of driving a liquid crystal display device comprising the steps of:

~~displaying an image with an n-bit digital image signal (n is an integer, where 2□n),~~

~~wherein the liquid crystal display device comprises a source signal line driver circuit, a gate signal line driver circuit, and a plurality of pixels,~~

~~wherein in the source signal line driver circuit, a sampling pulse is output from a shift register and input to a latch circuit,~~

generating a sampling pulse in a shift register;

inputting the sampling pulse to a latch circuit;

~~wherein in the latch circuit, the digital image signal is held in accordance with the sampling pulse, and the held digital image signal is written in to a source signal line,~~

inputting an n bit digital image signal (n is an integer, where 2 ≤n) in the latch circuit;

holding the n bit digital image signal in accordance with the sampling pulse;

outputting the n bit digital image signal from the latch circuit into a source signal line;

~~wherein in the gate signal line driver circuit, a gate signal line selection pulse is output to select a gate signal line, and~~

selecting a gate signal line in accordance with a gate signal line selection pulse;

~~wherein in respective plurality of pixels, in a row where the gate signal line is selected, write in of an n bit digital image signal input from the source signal line to the storage circuit, and reading of the n bit digital image signal stored in the storage circuit is performed~~

inputting the n bit digital image signal from the source signal line to a plurality of pixels, in a row where the gate signal line is selected;

selecting a storage circuit in the plurality of pixels;

writing the n bit digital image signal into the storage circuit via a write-in transistor; and

performing the n bit digital image signal read from the storage circuit via a read transistor.

47. (**Currently Amended**) A method according to claim 46, wherein in a display period of a still image, the source signal line driver circuit is stopped, and ~~by repeatedly reading~~ the n bit digital image signal stored in the storage circuit is repeatedly read to display the still image.

48. (**Previously Presented**) A method according to claim 46, wherein said method of driving the liquid crystal display device is used in an electronic device.

49. (**Original**) A method according to claim 48, wherein the electronic device is selected from the group consisting of a television, a personal computer, a portable terminal, a video camera or a head mount display.

50. (**Currently Amended**) A method of driving a liquid crystal display device ~~**displaying an image with an n bit digital image signal (n is an integer, where 2□n),**~~ comprising the steps of:

~~**wherein the liquid crystal display device comprises a gate signal line driver circuit, and a plurality of pixels,**~~

~~**wherein in the source signal line driver circuit, a sampling pulse is output from a shift register and input to a latch circuit,**~~

generating a sampling pulse in a shift register;

inputting the sampling pulse to a latch circuit;

~~**wherein in the latch circuit, the digital image signal is held in accordance with the sampling pulse, and the held digital image signal is written in to the source signal line,**~~

inputting an n bit digital image signal (n is an integer, where 2 ≤n) in the latch circuit;

holding the n bit digital image signal in accordance with the sampling pulse;

outputting the n bit digital image signal from the latch circuit into a source signal line;

~~**wherein in the gate signal line driver circuit, a gate signal line selection pulse is output and the gate signal lines are selected sequentially from the first row, and**~~

selecting a gate signal line sequentially from the first row in accordance with a gate signal line selection pulse;

~~**wherein in the plurality of pixels, write in of the n bit digital image signal sequentially from the first row is performed**~~

inputting the n bit digital image signal from the source signal line to a plurality of pixels, in a row where the gate signal line is selected;

selecting a storage circuit in the plurality of pixels;

writing the n bit digital image signal into the storage circuit via a write-in transistor; and

performing the n bit digital image signal read from the storage circuit via a read transistor.

51. (**Currently Amended**) A method according to claim 50, wherein in a display period of a still image, the source signal line driver circuit is stopped, and ~~**by repeatedly reading**~~ the n bit digital image signal stored in the storage circuit is repeatedly read to display the still image.

52. (**Previously Presented**) A method according to claim 50, wherein said method of driving the liquid crystal display device is used in an electronic device.

53. (**Original**) A method according to claim 52, wherein the electronic device is selected from the group consisting of a television, a personal computer, a portable terminal, a video camera or a head mount display.

54. (**Currently Amended**) A method of driving a liquid crystal display device ~~**displaying an image with an n bit digital image signal (n is an integer, where 2□n),**~~ comprising the steps of:

~~**wherein the liquid crystal display device comprises a gate signal line driver circuit, and a plurality of pixels,**~~

~~**wherein in the source signal line driver circuit, a sampling pulse is output from a shift register and input to a latch circuit,**~~

generating a sampling pulse in a shift register;

inputting the sampling pulse to a latch circuit;

~~**wherein in the latch circuit, the digital image signal is held in accordance with the sampling pulse, and the held digital image signal is written in to the source signal line,**~~

inputting an n bit digital image signal (n is an integer, where 2 ≤n) in the latch circuit;

holding the n bit digital image signal in accordance with the sampling pulse;

outputting the n bit digital image signal from the latch circuit into a source signal line;

~~**wherein in the gate signal line driver circuit, a gate signal line selection pulse is output by specifying an arbitrary row of the gate signal lines, and**~~

selecting a gate signal line arbitrary in accordance with a gate signal line selection pulse;

~~wherein in the plurality of pixels, write in of the n bit digital image signal is performed in an arbitrary row where the gate signal line is selected.~~

inputting the n bit digital image signal from the source signal line to a plurality of pixels, in a row where the gate signal line is selected;

selecting a storage circuit in the plurality of pixels;

writing the n bit digital image signal into the storage circuit via a write-in transistor; and

performing the n bit digital image signal read from the storage circuit via a read transistor, and

55. (**Currently Amended**) A method according to claim 54, wherein in a display period of a still image, the source signal line driver circuit is stopped, and ~~by repeatedly reading~~ the n bit digital image signal stored in the storage circuit is repeatedly read to display the still image.

56. (**Previously Presented**) A method according to claim 54, wherein said method of driving the liquid crystal display device is used in an electronic device.

57. (**Original**) A method according to claim 56, wherein the electronic device is selected from the group consisting of a television, a personal computer, a portable terminal, a video camera or a head mount display.

58. (**Previously Presented**) A device according to claim 11, wherein m > 1.

59. (**Previously Presented**) A device according to claim 21, wherein m > 1.

60. (**Previously Presented**) A device according to claim33, wherein m > 1.